

III-V-on-silicon integrated micro - spectrometer for the 3 μm wavelength range

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Abstract: A compact (1.2 mm²) fully integrated mid-IR spectrometer operating in the 3 μm wavelength range is presented. To our knowledge this is the longest wavelength integrated spectrometer operating in the important wavelength window for spectroscopy of organic compounds. The spectrometer is based on a silicon-on-insulator arrayed waveguide grating filter. An array of InAs_{0.91}Sb_{0.09} p-i-n photodiodes is heterogeneously integrated on the spectrometers output grating couplers using adhesive bonding. The spectrometer insertion loss is less than 3 dB and the waveguide-referred responsivity of the integrated photodiodes at room temperature is 0.3 A/W.

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1. Introduction

While silicon photonic integrated circuits are mainly targeting optical communication applications, the use of the platform is currently also being considered for optical sensing applications [1]. Many gases and bio-molecules absorb strongly in the mid-infrared (2-12 μm) wavelength range. Organic compounds have characteristic absorption features in the 3 - 4 μm wavelength range [2], and the detection and analysis of these compounds is of great importance for many practical applications. Both laser-based spectroscopy and dispersive spectrometers can be used for this purpose. While laser-based systems excel in terms of sensitivity and selectivity, such systems are often very expensive (need for a mid-IR tunable laser) and not rugged. Therefore there is an interest in dispersive spectrometers using a broadband light source. A number of discrete opto-electronic light emitters and photodetectors have been demonstrated to realize such spectroscopic systems in the 3 - 4 μm wavelength range [3–7]. The integration of such components on a photonic integrated circuit is essential for the miniaturization and cost reduction of such spectroscopic sensors. As a waveguide platform, silicon-on-insulator (SOI) stands out for these applications because of the mature fabrication processes, large volume fabrication potential and the fact that compact photonic integrated circuits can be realized. In our previous work we have demonstrated passive SOI spectrometers operating over a wide wavelength range, from 1.5 μm till 3.85 μm [8–11]. The integration of GaInAsSb-based p-i-n photodiodes with a cut-off wavelength of 2.65 μm on this platform was also demonstrated [12–14]. Also MEMS-based spectrometers for the mid-infrared wavelength range have been reported [15]. However, in order to address the industrially relevant detection of organic compounds the spectrometer operation needs to be extended to the 3 - 4 μm wavelength range. Also, in order for the system to remain compact and have low power consumption, room temperature operation of the system is required. In this paper we demonstrate to our knowledge the longest wavelength integrated spectrometer on the SOI waveguide platform, operating at 3.8 μm at room temperature. This is

specifically useful for the detection of carboxylic acids, but the operational wavelength range of the silicon spectrometer can also easily be brought down to e.g. address hydrocarbons in the 3.3 - 3.5 μm wavelength range [16]. This is realized through the heterogeneous integration of an array of InAsSb p-i-n photodiodes on an SOI spectrometer. In order to improve the sensitivity of the spectrometer at room temperature, special care is taken to passivate the photodetectors to reduce the dark current. Also, lock-in detection is used to enhance the sensitivity.

2. Design and simulation

A silicon-on-insulator arrayed waveguide grating (AWG) structure is used as a spectrometer. The design of the arrayed waveguide grating spectrometer is presented in [10]. It is implemented on a SOI wafer with a 380 nm silicon (220 nm crystalline silicon + 160 nm poly-silicon) device layer thickness and 2 μm buried oxide layer thickness. The waveguides are etched 160 nm deep and are cladded with SiO_2 . The AWG is designed for TE polarized light with a center wavelength of 3.8 μm . The AWG has six channels with a designed channel spacing of 9.6 nm. The input and output ports of the AWG are connected to grating couplers (etched 230 nm deep) for vertical interfacing with optical fiber and the photodiode array. Further details about the design and the layout parameters can be found in [10]. For the integration of the photodiodes we chose a grating-based coupling scheme because it is more fabrication tolerant as compared to other schemes like butt coupling or evanescent coupling. Figure 1 illustrates the grating-based coupling scheme where the light in the fundamental silicon waveguide mode is diffracted upwards to the III-V photodiode bonded on the grating coupler. The directionality of the coupler (i.e. the ratio of the optical power diffracted upwards to the total diffracted power) should therefore be maximized. The thickness of the grating bottom cladding (i.e. the buried oxide layer in this case) and the top cladding (i.e. SiO_2 /DVS-BCB where the DVS-BCB is used to bond the III-V epitaxial stack to the silicon photonic IC) determine the directionality.

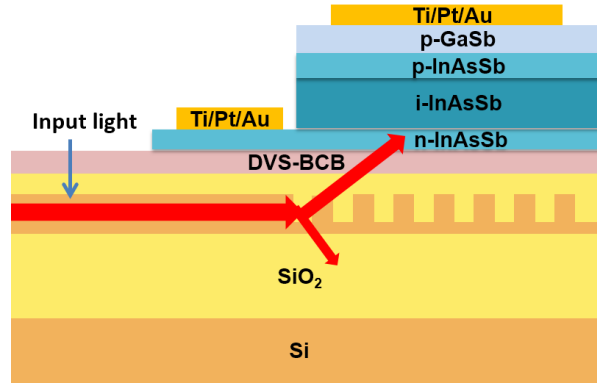


Fig. 1. Schematic view of the grating-based coupling scheme.

Figure 2 shows a full-vectorial two-dimensional calculation of the absorption in the intrinsic region of the bonded III-V photodiode as a function of the grating top and bottom cladding thickness. The silicon diffraction grating has a period of 2 μm , a duty cycle of 50% and is etched 230 nm deep. This simulation assumes a III-V stack consisting of 250 nm n-doped $\text{InAs}_{0.91}\text{Sb}_{0.09}$, 1000 nm intrinsically doped $\text{InAs}_{0.91}\text{Sb}_{0.09}$, 50 nm of p-doped $\text{InAs}_{0.91}\text{Sb}_{0.09}$ and 50 nm of p-doped GaSb as used in the experiment. As accurate data on the absorption coefficient of $\text{InAs}_{0.91}\text{Sb}_{0.09}$ is not available in the wavelength range of interest, 5000 cm^{-1} is used in the simulation, which is a reasonable assumption for a direct bandgap III-V material near

the band edge [17]. The buried oxide thickness in our photonic integrated circuit technology is fixed at 2000 ± 50 nm. A minimum upper cladding thickness of 800 nm is used to isolate the silicon waveguide mode from the environment. For an optimal top-cladding thickness of $1.3 \mu\text{m}$ and a buried oxide thickness of $2 \mu\text{m}$, about 25% of the incoming light gets absorbed in the intrinsic InAsSb layer.

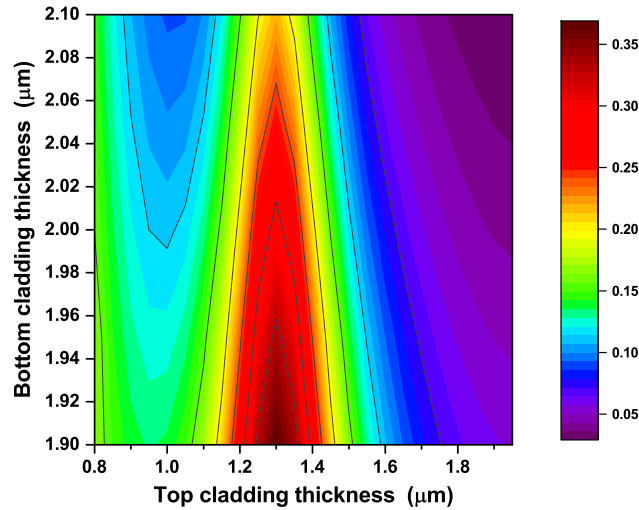


Fig. 2. 2D full-vectorial simulation of the fraction of power that is absorbed in the intrinsic region of p-i-n photodiode as a function of bottom and top cladding thickness.

3. Device fabrication

Fabrication of the SOI waveguide circuits is carried out in imec's CMOS pilot line using an advanced passives process flow [10]. At the end of the SOI chip fabrication a thick top cladding of SiO_2 is deposited and planarized to leave 800 nm SiO_2 on top of waveguides. This planarization serves three purposes. Firstly it improves the uniformity of the DVS-BCB bonding of the photodetector array. Secondly, as DVS-BCB (being a hydrocarbon) absorbs considerably in the $3 \mu\text{m}$ wavelength range [13], this 800 nm SiO_2 avoids the overlap of the silicon waveguide mode with the DVS-BCB. Lastly, the 800 nm SiO_2 on top of the waveguides serves as a protection layer for the underlying integrated waveguide circuits during the photodiode array fabrication. The GaSb-based III-V epitaxial layer stack used for the photodiode array is grown by solid-source Molecular Beam Epitaxy (MBE) in a reactor equipped with both As- and Sb-valved cracker cells and with conventional element-III cells. Be and Te were used as p- and n-type dopants. The substrates are on-axis (001) oriented n-type GaSb. After substrate de-oxidation at 550°C , a GaSb buffer layer was first grown at 500°C . Then, the temperature was decreased to 450°C to grow $0.5 \mu\text{m}$ of $\text{InAs}_{0.91}\text{Sb}_{0.09}$ to be used as an etch stop layer when removing the substrate in the integration process. Then, the p-i-n junction was defined as follows. First, a 50-nm-thick GaSb and a 50 nm thick $\text{InAs}_{0.91}\text{Sb}_{0.09}$ layers were grown as the p-zone (doping level 10^{18} cm^{-3}). The p-type GaSb layer serves as a low-resistance contact layer. Then, an unintentionally doped $1 \mu\text{m}$ thick $\text{InAs}_{0.91}\text{Sb}_{0.09}$ layer was grown as the absorption region. Finally, an n-type (10^{18} cm^{-3} doping level) 250-nm-thick $\text{InAs}_{0.91}\text{Sb}_{0.09}$ layer was grown. For the III-V-to-SOI bonding, a DVS-BCB:Mesitylene solution (40% DVS-BCB 3022-35 by volume) is used, resulting in a 300 nm thick bonding layer. After spin coating the

chip is pre-baked at 150°C for 5 minutes to evaporate residual mesitylene. The InAsSb detector die ($\sim 4 \text{ mm} \times 5 \text{ mm}$) is then bonded in vacuum ($4 \times 10^{-4} \text{ mbar}$) using a Karl Suss Microtech CB6L wafer bonder. The DVS-BCB is hard baked at 250°C during 1 hr. After bonding, the 500 μm thick GaSb substrate is lapped down to $\sim 75 \mu\text{m}$. The remaining GaSb substrate is then removed by wet etching with a $\text{HF}:\text{CrO}_3$ solution, until the etch stop layer ($\text{InAs}_{0.91}\text{Sb}_{0.09}$) is reached. The etch stop layer is then removed using a citric acid: H_2O_2 (2:1 v/v) solution. Now the thin film of III-V is ready for photodiode processing, which starts with the definition of the photodiode mesas (30 $\mu\text{m} \times 45 \mu\text{m}$), lithographically aligned to the output grating couplers. The mesa is defined using a tartaric acid-based solution to remove the GaSb p-contact layer. Citric acid: H_2O_2 (2:1 v/v) is used to reach the bottom n-contact of the p-i-n structure. Ti (2 nm) / Pt (35 nm) / Au (100 nm) p-type and n-type contacts are then deposited using e-beam evaporation. DVS-BCB is spin-coated and cured at 250°C for one hour to passivate the detectors. Then vias are etched in the DVS-BCB using dry etching to access the top and bottom contact pads. Finally, Ti (40 nm) / Au (500 nm) contacts are deposited to probe the detectors. Figure 3 shows a microscope image of the integrated spectrometer as well as a SEM cross-section of the photodiode/SOI interface. The size of AWG is 1.1 mm \times 0.78 mm and the overall spectrometer (AWG and output waveguides with photodiodes) occupies an area of 1.2 mm².

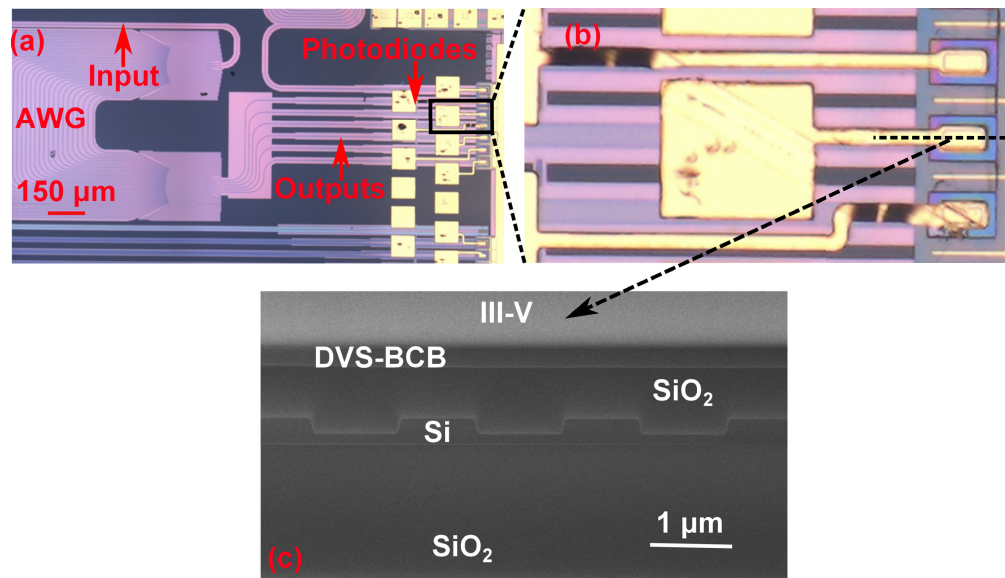


Fig. 3. (a) Microscopic image of complete fabricated device, (b) close-up of a single heterogeneously integrated photodiode and (c) SEM cross-section of the photodiode. The SEM image is taken on the dotted line.

4. Spectrometer characterization

First, the integrated photodiodes are characterized electrically by measuring the IV curves at room temperature using a Keithley 2400 source meter. The DVS-BCB passivation of the photodiodes proved to be essential for the spectrometer operation. Figure 4(a) shows the room temperature IV characteristics of a 90 μm by 90 μm photodiode before (black) and after (blue) passivation. Before passivation the device shows no rectifying behavior, which substantially improves after DVS-BCB passivation. This is attributed to a strong sidewall leakage current without proper passivation. The average room temperature dark current of the fabricated pho-

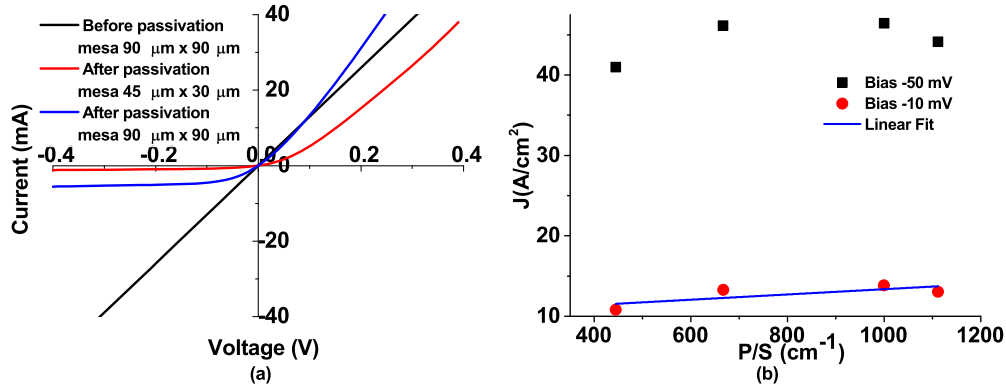


Fig. 4. (a) Effect of DVS-BCB passivation on room temperature IV-characteristics of the photodiode, (b) Dark current density versus perimeter to surface area ratio for different photodiode mesa sizes.

todiodes on the SOI spectrometer (mesa size $30 \mu\text{m} \times 45 \mu\text{m}$) is around $600 \mu\text{A}$ and $170 \mu\text{A}$ at bias voltages of -50 mV and -10 mV respectively. To investigate the origin of the high dark current even after DVS-BCB passivation the IV curves of photodiodes with different mesa sizes were measured. Figure 4(b) shows the dark current density at room temperature as a function of the perimeter over surface area ratio of the photodiode mesa. The y-intercept of this graph shows a bulk dark current density contribution of 10.1 A/cm^2 at 10 mV reverse bias. For the integrated detector mesa size of $30 \mu\text{m} \times 45 \mu\text{m}$ this translates into $136 \mu\text{A}$ of diode dark current and a $34 \mu\text{A}$ side-wall leakage current. In this first implementation a homogeneous p-i-n structure is used. In literature [13, 14] it is shown that by using high bandgap barriers the bulk leakage can be reduced significantly. To suppress the sidewall leakage current a better passivation like in [14] can be applied.

Next, the integrated spectrometer is characterized optically. The measurement setup is shown in Fig. 5. Mid-infrared light from an OPO system (Aculight 2400 model) is chopped and coupled to single-mode ZrF₄ fiber after which it is vertically coupled to the chip under a 15° angle. The polarization is adjusted to TE using a Babinet-Soleil compensator in free space. To compensate for slow fluctuations of the OPO output power, the photodiode response is normalized using a thermopile detector (Thorlabs S401C), which monitors a fraction of the output power in free space. The integrated photodiode response is measured using a pre-amplifier from

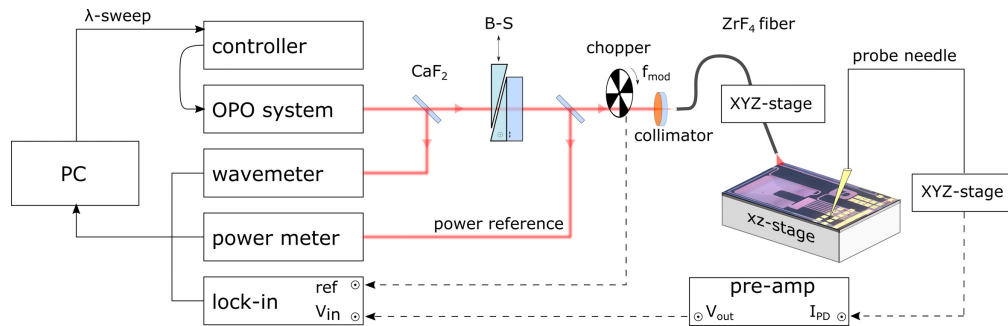


Fig. 5. Schematic of the measurement setup used to characterize the integrated spectrometer.

Infrared Associates (InSb-1000) at zero bias. To increase the signal to noise ratio, the output of the pre-amplifier is connected to a lock-in amplifier (SR 830). The wavelength of the OPO is swept by controlling the crystal position using a stepper motor and adjusting the intra-cavity etalon angle. The wavelength is measured using a Bristol 621 wavemeter and the wavelength step is approximately 1 nm. The output of the lock-in amplifier and the wavemeter are read out simultaneously using a PC. To remove any measurement fluctuations, 10 readings from the lock-in amplifier were collected per wavelength point. These readings are then averaged and normalized with respect to the average of the reference power measured from the thermopile detector.

The measurement results are illustrated in Fig. 6. Good uniformity between the 6 channels of the spectrometer is obtained. The cross talk of the integrated spectrometer is 16 dB. This is slightly worse than the crosstalk of the previously reported passive spectrometer (20 dB) [10]. This is attributed to the increase in phase noise in the arrayed waveguide grating due to the processing of the photodetectors. The system responsivity (defined as ratio of the measured

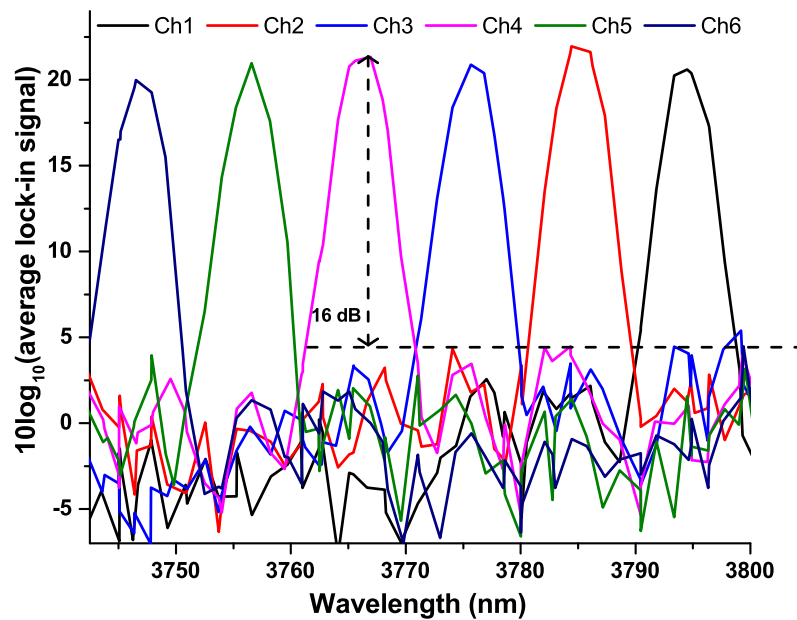


Fig. 6. Measured photoresponse of the integrated spectrometer.

photocurrent to the optical power in fiber) is 1.1 mA/W. The system responsivity is relatively low mainly because of the low fiber-to-chip coupling efficiency of the grating couplers (measured to be -20 dB). Taking into account the insertion loss of the AWG (3 dB) and the waveguide losses in the circuit (5 dB/cm) an on-chip photodiode responsivity of 0.3 A/W is deduced. This on-chip responsivity corresponds to a quantum efficiency of around 10 %, which matches well to the simulated value in Fig. 2 for a top cladding thickness of around 1.1 μm .

In order to improve the on-chip responsivity, several approaches can be followed. The system responsivity can be improved by using an optimized silicon waveguide to photodiode grating coupler. Using a grating with 310 nm etch depth, 2.4 μm period and 50% duty cycle can improve the on-chip responsivity by a factor of 2. Another way of improving the on-chip responsivity is to improve the directionality (i.e. fraction of power diffracted upwards) of the grating coupler by using a bottom metal mirror [18]. This can be realized by local silicon substrate

removal (KOH-based wet etching or Bosch deep RIE etching) and depositing a metal mirror.

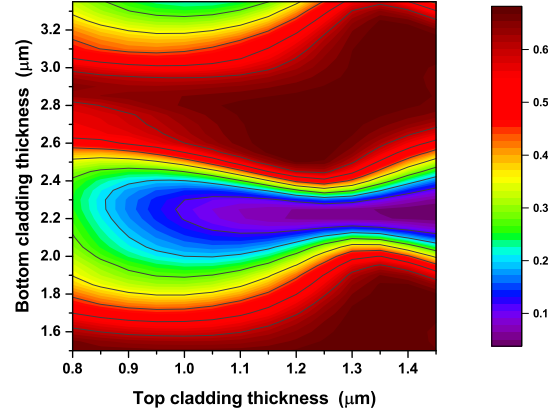


Fig. 7. 2D full-vectorial calculation for improvement in detector absorption by using a bottom metal mirror (grating parameters: period 2 μm , etch depth 230 nm and duty cycle 50%).

Figure 7 shows a simulation result similar to Fig. 2 but now assuming a bottom metal mirror. As can be seen from Fig. 7, this approach is also very fabrication tolerant as there is a large window around a bottom cladding thickness of 2.8 μm and a top cladding thickness of 1.3 μm where the absorption stays above 60%.

The Johnson noise limited specific detectivity D^* of the integrated photodetectors is linked to the zero bias resistance area product (R_oA) and responsivity (R_{pd}) by the following equation,

$$D^* = R_{pd} * \sqrt{\frac{R_oA}{4kT}} \quad (1)$$

where k is the Boltzman constant and T is the absolute temperature. With an R_oA value of $7.4 \times 10^{-4} \Omega \text{ cm}^2$ at room temperature as calculated from Fig. 4(b) and a measured responsivity of 0.3 A/W the specific detectivity D^* is $6.4 \times 10^7 \text{ cmHz}^{1/2}\text{W}^{-1}$. D^* can be improved by increasing the responsivity as explained above and using the dark current reduction strategies as discussed above. Obviously low temperature operation also leads to higher detectivity.

5. Conclusion

In this paper we demonstrate, to our knowledge, the longest wavelength integrated microspectrometer, addressing the industrially relevant 3 - 4 μm wavelength range. This is realized by the heterogeneous integration of an $\text{InAs}_{0.91}\text{Sb}_{0.09}$ based photodiode array on an SOI spectrometer. The heterogeneous integration technology presented here can also be applied to realize broadband light sources on-chip, paving the way for fully integrated spectroscopic sensing systems on-chip.

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